



Article

Area-Efficient Universal Code Generator for Multi-GNSS Receivers

Minsu Kim, Jiwoon Park, Gwanghee Jo  and Hoyoung Yoo * 

Department of Electronics Engineering, Chungnam National University, Daejeon 34134, Korea; mskim.cas@gmail.com (M.K.); jwpark.cas@gmail.com (J.P.); j_ghee@cnu.ac.kr (G.J.)

* Correspondence: hyyoo@cnu.ac.kr

Abstract: Although conventional global navigation satellite systems (GNSS) receivers were originally designed for single signals, studies on multi-signal receiver design have recently been actively conducted to achieve high accuracy, precision, and reliability. However, in order for a multi-signal receiver to support various codes, the receiver should support the generation of individual codes. Therefore, the resulting problem of increased complexity must be solved. This paper proposes a hardware structure for an area-efficient linear feedback shift register (LFSR)-based multi-frequency universal code generator. Whereas the existing universal code generators were configured so that feedback polynomials, output registers, and initial values can be selected by placing read-only memories (ROMs), multiplexers (MUXs), and exclusive ORs (XORs) by register bit, in the case of the proposed universal code generator; the circuit was implemented by applying the hardwiring technique to those register bits that have fixed values. According to the results of field programmable gate array (FPGA) implementation, the proposed LFSR-based universal code generator can improve look up table (LUT) by up to 37% and register by up to 78% when compared to conventional code generators, and LUT by up to 36% when compared to the previous universal code generator. Therefore, the proposed universal code generator is a good candidate for implementing multi-frequency receivers to achieve high precision and high reliability.



Citation: Kim, M.; Park, J.; Jo, G.; Yoo, H. Area-Efficient Universal Code Generator for Multi-GNSS Receivers. *Electronics* **2021**, *10*, 2485. <https://doi.org/10.3390/electronics10202485>

Academic Editor: Athanasios Kanatas

Received: 8 September 2021

Accepted: 8 October 2021

Published: 13 October 2021

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Keywords: global navigation satellite system; universal code generator; linear feedback shift register; hardwiring technique

1. Introduction

A global navigation satellite system (GNSS) is a positioning and time determination system that supports global navigation services using satellite constellations [1]. The position and time information provided by GNSS is widely applied in the fields of national defense, finance, communications, and medicine, and its application has recently spread to various other fields such as autonomous driving and smart devices [2,3]. Representative GNSS satellite constellations include the U.S. Global Positioning System (GPS), Russia's GLONASS, China's BeiDou Navigation Satellite System (BDS), and the EU's Galileo, and they have been continuously researched and developed with a view to improving the accuracy and use of satellite signals. GNSS signals are transmitted in the frequency bands determined by the satellites. For example, GPS signals, which are the most representative GNSS signals, consist of L1C/A and L1C signals in the L1 (1575.42 MHz) band, L2C signals in the L2 (1227.60 MHz) band, and L5 signals in the L5 (1176.45 MHz) band [4].

To identify visible satellites among signals received from multiple satellites and to extract navigation messages, GNSS receivers use the pseudo random noise (PRN) code [4]. The PRN code is characterized by having high correlation values for two same PRN codes, and low correlation values for two different PRNs codes. By using this characteristic of the PRN code, GNSS receivers can distinguish signals from different satellites. To maintain the correlation characteristic of the PRN code, it is important to carefully design the code. Note that since most GNSS satellite constellations employ CDMA, a different PRN is assigned to each satellite. Exceptionally, GLONASS L1OF and L2OF uses FDMA so that different

satellites of GLONASS share the same PRN, and the satellites are distinguished using frequency difference.

Although conventional GNSS receivers have generally been designed for single signals, studies on multi-signal receiver design have recently been actively conducted to achieve high accuracy, precision, and reliability [5–7]. In general, multi-signal receivers can be divided into multi-GNSS receivers that receive multiple GNSS signals of a single frequency band, multi-frequency receivers that receive single GNSS signals of multiple frequency bands, and multi-GNSS multi-frequency receivers that receive multiple GNSS signals of multiple frequency bands. However, in order for a multi-signal receiver to support various codes, the receiver should support the generation of individual codes. Therefore, the resulting problem of increased complexity must be solved. This paper proposes a structure for a universal code generator that can generate multiple codes by sharing hardware resources. With this foregoing structure, the optimized implementation of multi-signal receivers can be supported.

2. Background

The PRN code has high correlation values for the same PRN codes and low correlation values for different PRN codes. To generate a PRN code that has the correlation characteristic, there are three methods: a linear feedback shift register (LFSR), a Legendre sequence, and a memory code [5]. The LFSR is a design method using linear combinations of shift registers, the Legendre sequence is a method based on a mathematical sequence, and the memory code is a method of storing and reading predetermined sequences in memory. Table 1 shows the frequency bands and PRN code generation methods for representative GNSS signals. As shown in Table 1, most of the signals are generated based on the LFSR, while the GPS L1C signals [8] and the BDS B1C signals [9] are generated using the Legendre sequence, and the code of the Galileo E1 signals [10] is generated based on the memory code. This paper focuses on a structure that can support various signals by sharing hardware for LFSR, which is the most widely applied. As shown in Figure 1, the LFSR-based code generator basically consists of shift registers, a Feedback Tap circuit, an Initial read-only memory (ROM), and an output circuit. The LFSR-based PRN generation method for GNSS is subdivided into M-sequence, gold code, and kasami code according to the detailed configuration of LFSR [6].

Table 1. Summary the code generation method of GNSS signals [8–22].

GNSS	Frequency Band	Signal	Code Structure	Code Type
GPS	L1	L1C/A	LFSR (10b, 10b)	Gold code
		L1C	Legendre sequence	Weil code
	L2	L2C (L2CM/ L2CL)	LFSR (27b)	M-sequence
	L5	L5 I	LFSR (13b, 13b)	Gold code
		L5 Q	LFSR (13b, 13b)	Gold code
BDS	B1	B1I	LFSR (11b, 11b)	Gold code
	L1	B1C	Legendre sequence	Weil code
	B2	B2I	LFSR (11b, 11b)	Gold code
	L5	B2A (B2ad/B2ap)	LFSR (13b, 13b)	Gold code
	B3	B3I	LFSR (13b, 13b)	Gold code

Table 1. Cont.

GNSS	Frequency Band	Signal	Code Structure	Code Type
GLONASS	L1	L1OF	LFSR (9b)	M-sequence
		L1OC (L1OCd/L1OCp)	LFSR (10b, 10b/12b, 6b)	Gold code/Kasami code
	L2	L2OF	LFSR (9b)	M-sequence
		L2OC (L2OCp)	LFSR (14b, 7b)	Kasami code
	L3	L3OC (L3OCd/L3OCp)	LFSR (14b, 7b)	Kasami code
Galileo	E1	E1	Memory code	Memory code
	E5	E5a (E5a-I/E5a-Q)	LFSR (14b, 14b)	Gold code
		E5b (E5b-I/E5b-Q)	LFSR (14b, 14b)	Gold code

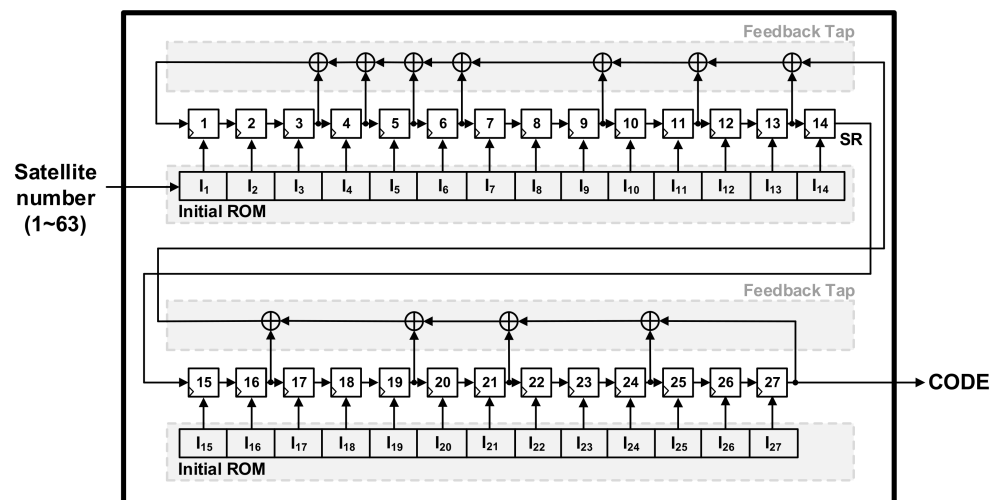


Figure 1. Conventional code generator architecture of GPS L2C signal [11].

2.1. M-Sequence

The M-sequence method that has a maximum length sequence (MLS) is a method of generating a sequence with the length of $2^N - 1$, which is the maximum length that can be generated, through linear feedback using a shift register of length N [22,23]. The PRN code of the M-sequence method has the property of having the highest correlation value at zero lag in the case of autocorrelation and almost no correlation value in the case of cross correlation. Signals that use the M-sequence code include GPS L2C [11], GPS L5 I [12], GPS L5 Q [12], GLONASS L1OF [13], and GLONASS L2OF signals [13].

As shown in Table 1, the code generator for GPS L2C signals is a representative example of M-sequence code generators [11]. The codes of GPS L2C signals include the L2CM code and the L2CL code, and both codes use the same code generator structure. Figure 1 shows the architecture of the code generator for the GPS L2C signals converted into the Fibonacci LFSR. Please note that the code generator of GPS L2C signals has the structure of Galois LFSR in Interface Control Documents (ICD), but the structure can be converted into Fibonacci LFSR when it is used [24]. The code generator shown in Figure 1 consists of one 27-bit shift register, Feedback Tap, and Initial ROM. The feedback polynomial of the shift register is $f(x) = x^{27} + x^{24} + x^{21} + x^{19} + x^{16} + x^{13} + x^{11} + x^9 + x^6 + x^5 + x^4 + x^3 + 1$. The initial value designated for each satellite number is stored in Initial ROM. When the satellite number is input into the Initial ROM, the stored initial value is input into the shift register and operates. After the initialized LFSR value is moved linearly, the value of the shift register is updated through the feedback circuit and operates. At this time, the last register output becomes the

PRN code of the GPS L2C signal. The code generator shown in Figure 1 can support both the L2CM code and L2CL code. The L2CM code generates PRN codes that are 10,230 chips long, and L2CL code generates PRN codes that are 767,250 chips long.

2.2. Gold Code

The gold code generator consists of two N -bit shift registers with different feedback polynomials and initial values. The two N -bit shift registers have two different M -sequences of equal length as outputs. Gold codes with lengths up to $2^N - 1$ are generated through the bitwise modulo sum of the two output sequences. Signals using gold codes include GPS L1C/A [14], BDS B1I [15], BDS B2I [15], BDS B2A [16], BDS B3I [17], GLONASS L1OCd [18], Galileo E5a [19], and Galileo E5b [19]. The two LFSR structures of the gold code generator are basically the same as the LFSR structure of the M -sequence generator structure shown in Figure 1, but instead of storing the initial value of the shift register in the ROM, a phase selector circuit that selectively determines the output according to the satellite number may be added [4]. Among the signals that use the gold code, the signals that use the phase selector are GPS L1C/A signals, BDS B1I and BDS B2I signals.

Figure 2 shows an example of a gold code generator that has the structure of a GPS L1C/A code generator [14]. The gold code generator shown in Figure 2 consists of 10-bit shift registers SR1 and SR2, Feedback Taps1/2, Initial ROMs 1/2, and a phase selector. The feedback polynomial of SR1 is $f(x) = x^{10} + x^3 + 1$, and the feedback polynomial of SR2 is $f(x) = x^{10} + x^9 + x^8 + x^6 + x^3 + x^2 + 1$. Each polynomial is implemented with Feedback Taps 1/2. The initial value information of the two shift registers is stored in Initial ROMs 1/2, and the stored initial values are set in shift registers SR1 and SR2. Furthermore, the phase selector selects the two register outputs determined for each satellite number from shift register SR2 to perform modulo-2 summing. In detail, the phase selector consists of as many multiplexers (MUXs) as shift registers, a Selection ROM that stores the multiplexers' control signals, and exclusive OR (XOR) logic. When a satellite number is input, two register outputs determined for each satellite number are selected due to the control signal information stored in the Selection ROM, and modulo-2 summing can be performed. Finally, the L1C/A code is generated with the last register output of shift register. SR1 and the modulo-2 sum of the output of the phase selector and has a length of 1023 chips.

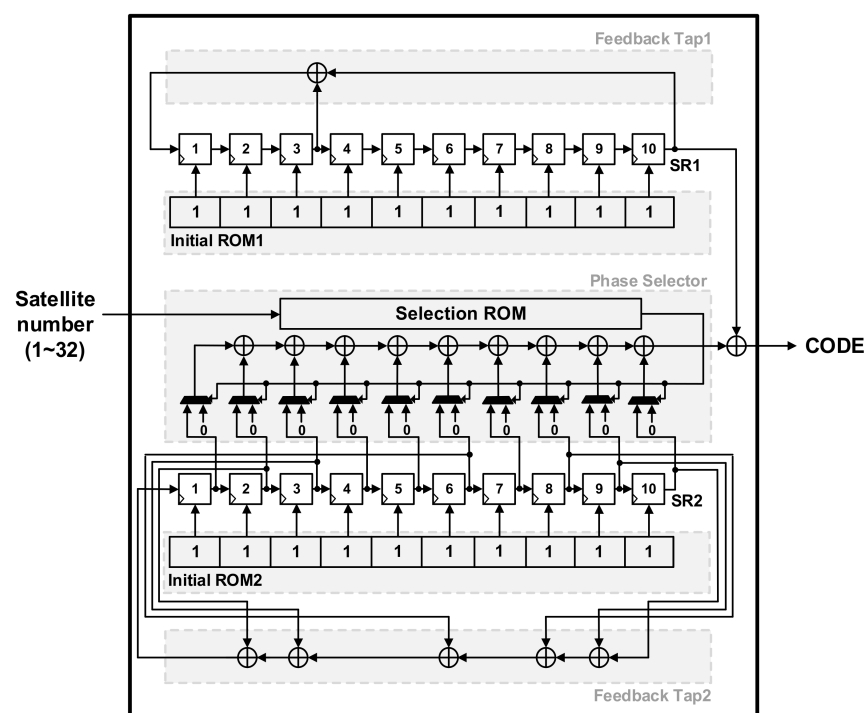


Figure 2. Conventional code generator architecture of GPS L1C/A signal [14].

2.3. Kasami Code

When compared with the gold code generator shown in Figure 2, the kasami code generator is identical in that it consists of two LFSRs but is different in that the length of the LFSR is different. In detail, the shift register of the kasami code generator uses an N -bit shift register and a half-length $N/2$ -bit shift register to generate the kasami code, which is $2^N - 1$ long at maximum. Signals that use the code type of the kasami code include GLONASS L1OCp [18], GLONASS L2OC [20] and GLONASS L3OC [21].

Figure 3 shows the GLONASS L2OC code generator, which is an example of a kasami code generator. The generator consists of a 14-bit shift register SR1, a 7-bit shift register SR2, Feedback Taps1/2, and Initial ROMs1/2 [20]. The feedback polynomial of SR1 shown in Figure 3 is $f(x) = x^{14} + x^{13} + x^8 + x^4 + 1$, and the feedback polynomial of SR2 is $f(x) = x^7 + x^6 + 1$. The initial value of SR1 and the initial value of SR2 are stored in Initial ROMs1/2, respectively, and in this case, the initial value of SR2 has different initial values by satellite number. When the predetermined feedback polynomial and initial value are set and operate, the outputs of the 14th register of shift register SR1 and the 7th register of shift register SR2 are modulo-2 summed to generate 10,230 chips long L2OCp code of GLONASS L2OC.

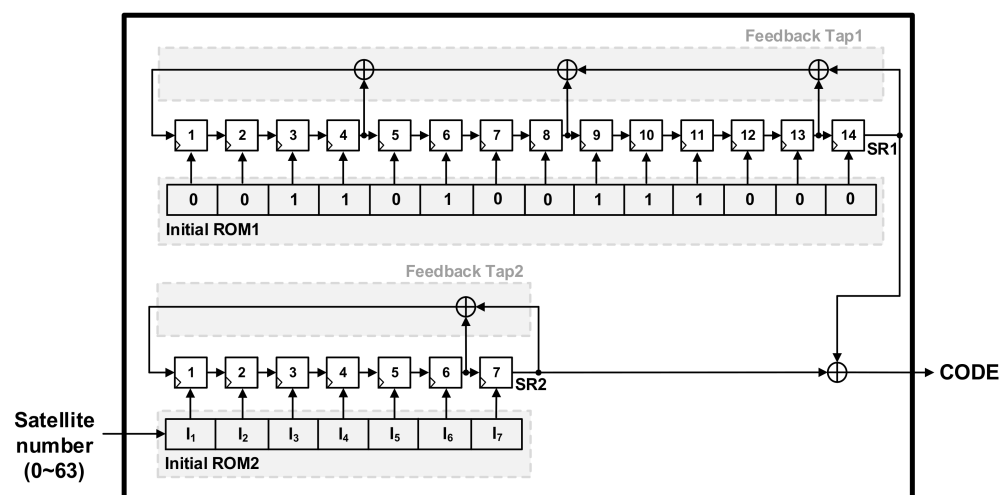


Figure 3. Conventional code generator architecture of GLONASS L2OC signal [20].

3. Previous Multi-Frequency Universal Code Generator

The characteristics of the LFSR-based code generator for generating the PRN code are determined by the length of the shift registers, the feedback polynomials, the initial values, and the output registers. The various types of LFSR-based code generators shown in Table 1 have their own values, which are described in their respective ICDs. A code generator structure that supports various codes is an essential element in the development of multi-signal receivers, which have been recently studied to improve accuracy, precision, and reliability. In addition, since the complexity of the code generator increases linearly by the number of supported codes, an efficient receiver structure must be studied without fail. Recently, [6] proposed an LFSR structure that can support multiple codes. The hardware was configured to share the shift register of the LFSR and to selectively determine different feedback polynomials, output registers, and initial values by code generator. Through the foregoing, multiple codes can be selectively generated with a single LFSR hardware device.

Figure 4 shows the hardware architectures of the previous multi-frequency universal code generators for signals using the LFSR-based code generators by GNSS. Figure 4 shows the hardware architectures of the previous LFSR-based multi-frequency universal code generators that can generate the codes of GPS signals, BDS signals, GLONASS signals, and Galileo signals, respectively. The previous multi-frequency universal code generators shown in Figure 4 commonly consist of shift registers SR1 and SR2, Feedback

Taps1/2, which set the feedback polynomial of each shift register, Initial ROMs1/2 that store the initial values of the two shift registers, and Output Taps1/2, which determine the output registers.

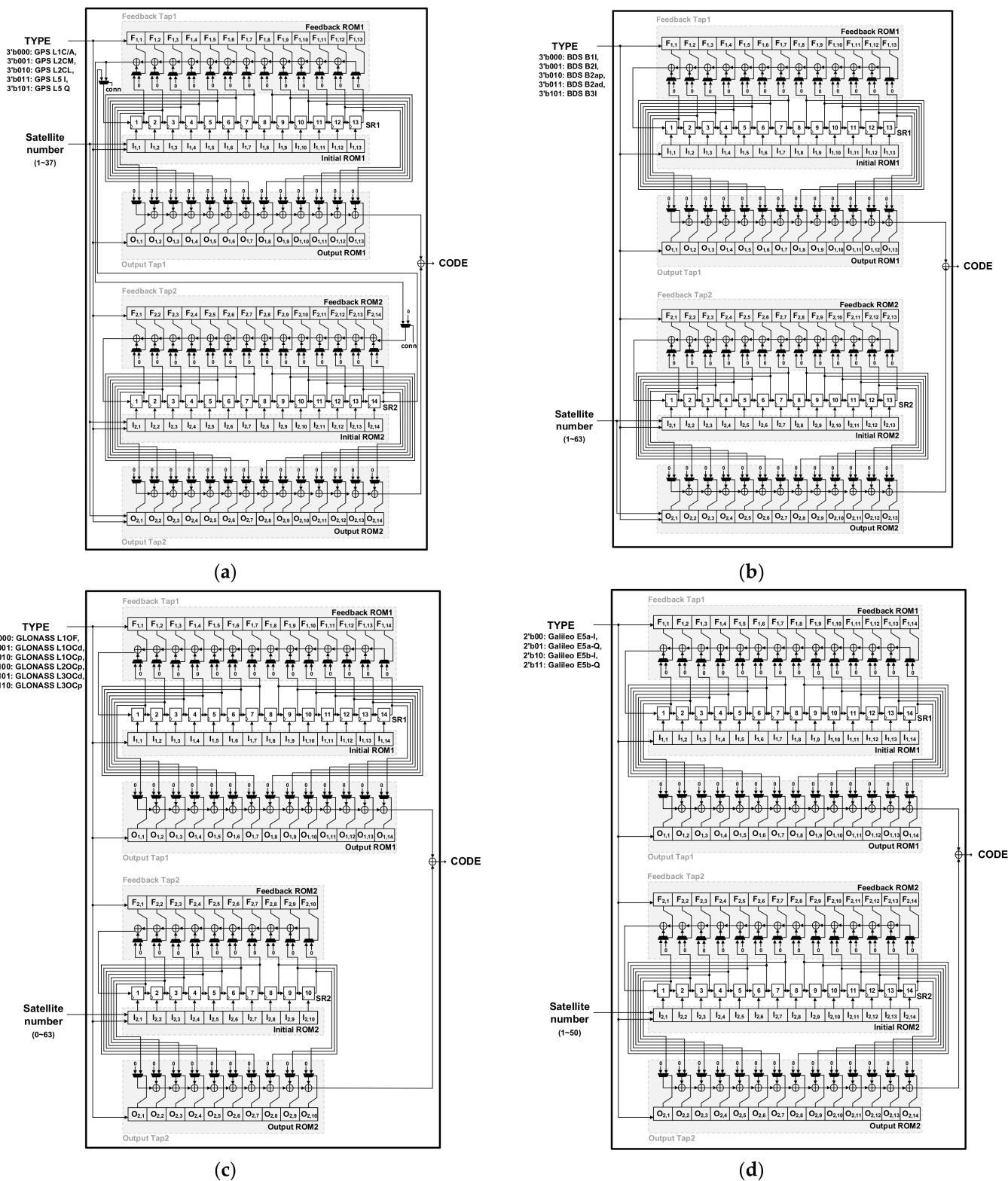


Figure 4. Previous multi-frequency universal code generator architectures [6] of each GNSS signal. (a) GPS. (b) BDS. (c) GLONASS. (d) Galileo.

The length of the shift register of previous multi-frequency universal code generators is determined by the length of the longest shift register among the shift registers of the code generators by signal. As shown in Table 1, the previous multi-frequency universal code generator for GPS signals shown in Figure 4a supports GPS L1C/A, GPS L2CM, GPS L2CL, GPS L5 I, and GPS L5 Q. Since the M-sequence-based code generator for GPS L2C signals requires the 27-bit shift register and the gold code-based code generator for GPS L5 signals requires the 13-bit, 13-bit shift registers, the two shift registers SR1 and SR2 were designed to be 13 bits and 14 bits, respectively. The control signal conn selectively determines the operations of M-sequence-based L2C signals and gold code-based L1C/A and L5 signals. As with the universal code generator for GPS signals, in the case of the previous multi-frequency universal code generator for BDS signals shown in Figure 4b, the BDS B2A and B3I signals, which use the maximum number of bit shift registers in the code generator, use 13-bit, 13-bit shift registers. Therefore, both SR1 and SR2 were designed to be 13 bits. In the case of the previous multi-frequency universal code generators for GLONASS signals shown in Figure 4c, since the GLONASS L2OC and L3OC signal code generators use 14-bit and 7-bit shift registers, respectively, and both code generators use 10-bit shift registers to generate the L1OCd code of the GLONASS L1OC signals, SR1 and SR2 are 14 bits and 10 bits, respectively, which are the maximum numbers of bits. Finally, in the case of the previous multi-frequency universal code generators for Galileo signals shown in Figure 4d, since the code generators for all signals use 14-bit, 14-bit shift registers, SR1 and SR2 are 14 bits and 14 bits.

As shown in Figure 4, in [6], the maximum length shift register was implemented, and ROM, MUX, and XOR circuits were configured so that feedback polynomials, output registers, and initial values different by code generator can be selectively determined. As many multiplexers as the number of bits of the shift register, as many XOR logics as (the number of bits of the shift register – 1), and Feedback ROMs1/2 and Output ROMs1/2 that store the multiplexers' control signals are used. Initial ROMs1/2 store the initial values determined by code, and the initial values are set in the shift registers connected according to the code types and satellite numbers. Therefore, each ROM needs as much width as the number of shift registers and as much depth as the supported (code types × the number of satellite numbers).

The code generators shown in Figure 4 can universally generate various types of codes with a single LFSR structure. The code type and the satellite number are received as inputs, the feedback polynomials, output registers and initial values of SR1 and SR2 are determined, and the generated PRN codes are output as codes. For example, in the case where the PRN code for satellite number 2 of the GPS L1C/A signals is generated using the code generators shown in Figure 4a, in order to set the feedback polynomials, Feedback Taps 1/2 receive the code type as an input, and $\{F_{1,13}, F_{1,12}, F_{1,11}, \dots, F_{1,1}\}$ is set to {000100000100}, and $\{F_{1,14}, F_{1,13}, F_{1,12}, \dots, F_{1,1}\}$ is set to {00001110100110}. In addition, to set the output registers, Output Tap1 receives the code type and $\{O_{1,13}, O_{1,12}, O_{1,11}, \dots, O_{1,1}\}$ is set to {000100000000}. Since Output Tap2 is affected by the satellite number, it receives code type and satellite number as inputs, and $\{O_{1,14}, O_{1,13}, O_{1,12}, \dots, O_{1,1}\}$ is set to {00000001000100}. Additionally, since Initial ROMs1/2 are affected by the satellite number, they receive the code type and satellite number as inputs, and $\{I_{1,13}, I_{1,12}, I_{1,11}, \dots, I_{1,1}\}$ is set to {000111111111}, and $\{I_{1,14}, I_{1,13}, I_{1,12}, \dots, I_{1,1}\}$ is set to {000011111111}. Therefore, the universal code generator structure presented in [6] can reduce hardware complexity because it can selectively generate various codes according to the given type and satellite number inputs.

4. Proposed Multi-Frequency Universal Code Generator

Although the previous universal code generators can generate various codes using a single LFSR, there are many unnecessary elements in the values stored by supported satellite signal. The proposed multi-frequency universal code generator is intended to remove the unnecessary elements to further reduce the complexity.

Whereas the previous universal code generator configured Initial ROMs, Feedback ROMs, and Output ROMs for all register bits so that they can operate selectively, the proposed universal code generator opened the bits that are not regularly used and directly connected the bits that are used regularly to remove unnecessary ROM, MUX, and XOR circuits. By applying the hardwiring technique, redundant hardware resources can be significantly reduced compared to previous multi-frequency universal code generators.

Tables 2–5 show summaries of the ROM values of the conventional code generators in binary numbers by GNSS signal. Commonly unused bits were expressed as 0, used bits as 1, and non-fixed bits as don't care X. According to the summaries, many bits are fixed to 0 and 1, so that a large number of hardware resources can be reduced by applying the hardwiring technique. Although the don't care X bits require ROM, MUX, and XOR identically to the existing hardware configuration, the shift registers corresponding to bit 0 can be configured by removing the ROM, MUX, and XOR and opening them. In the case of the shift registers corresponding to bit 1, the ROM and MUX can be removed and an XOR connection can be directly configured. Therefore, the more the fixed bits 0 and 1 exist, the more the unnecessary hardware resources can be removed.

Table 2. The fixed parameters of code generators for GPS signals.

Codes	Feedback ROM1 (13 bit)	Feedback ROM2 (14 bit)	Output ROM1 (13 bit)	Output ROM2 (14 bit)	Initial ROM1 (13 bit)	Initial ROM2 (14 bit)
L1C/A	0001000000100	00001110100110	0001000000000	0000xxxxxxxxxxx	0001111111111	0000111111111
L2CM	1001001010010	01010100111100	1000000000000	0000000000000	xxxxxxxxxxxxxxx	xxxxxxxxxxxxxxx
L2CL	1001001010010	01010100111100	1000000000000	0000000000000	xxxxxxxxxxxxxxx	xxxxxxxxxxxxxxx
L5 I	1101100000000	01100011101101	1000000000000	0100000000000	1111111111111	0xxxxxxxxxxxxxx
L5 Q	1101100000000	01100011101101	1000000000000	0100000000000	1111111111111	0xxxxxxxxxxxxxx
Summary	xx01x0x0x0xx0	0xxxxxxx1xx1xx	x0x0000000000	0x00xxxxxxxxxxx	xxxxxxxxxxxxxxx	xxxxxxxxxxxxxxx

Table 3. The fixed parameters of code generators for BDS signals.

Codes	Feedback ROM1 (13 bit)	Feedback ROM2 (14 bit)	Output ROM1 (13 bit)	Output ROM2 (14 bit)	Initial ROM1 (13 bit)	Initial ROM2 (14 bit)
B1I	0011111000001	0010110011111	0010000000000	00xxxxxxxxxxx	0001010101010	0001010101010
B2I	0011111000001	0010110011111	0010000000000	00xxxxxxxxxxx	0001010101010	0001010101010
B2ad	1010000010001	1110100010100	1000000000000	1000000000000	1111111111111	xxxxxxxxxxxxxxx
B2ap	1000001100100	1100011010001	1000000000000	1000000000000	1111111111111	xxxxxxxxxxxxxxx
B3I	1000000001101	1101101110001	1000000000000	1000000000000	1111111111111	xxxxxxxxxxxxxxx
Summary	x0xxxxxxxx0x	xxxxxxx1xxxx	x0x0000000000	x0xxxxxxxxxxx	xxx1x1x1x1x1x	xxxxxxxxxxxxxxx

Table 4. The fixed parameters of code generators for GLONASS signals.

Codes	Feedback ROM1 (14 bit)	Feedback ROM2 (10 bit)	Output ROM1 (14 bit)	Output ROM2 (10 bit)	Initial ROM1 (14 bit)	Initial ROM2 (10 bit)
L1OF	–	0100010000	–	0001000000	–	0111111111
L2OFF	–	0100010000	–	0001000000	–	0111111111
L1OCd	00001001000000	1101000100	00001000000000	1000000000	00000001001100	xxxxxx0000
L1OCp	00110010100000	0000100001	00100000000000	0000100000	00101000110000	0000xxxxxx
L2OCP	11000010001000	0001100000	10000000000000	0001000000	00011100101100	000xxxxxx1
L3OCd	11000010001000	0001100000	10000000000000	0001000000	00011100101100	000xxxxxx0
L3OCp	11000010001000	0001100000	10000000000000	0001000000	00011100101100	000xxxxxx1
Summary	xxxxx0xxx0x000	xx0xxx0x0x	x0x0x000000000	x00xx00000	00xxxx0xxxxx00	xxxxxxxxxxx

Table 5. The fixed parameters of code generators for Galileo signals.

Codes	Feedback ROM1 (13 bit)	Feedback ROM2 (14 bit)	Output ROM1 (13 bit)	Output ROM2 (14 bit)	Initial ROM1 (13 bit)	Initial ROM2 (14 bit)
E5a-I	10000010100001	10100011011000	10000000000000	10000000000000	11111111111111	xxxxxxxxxxxxxx
E5a-Q	10000010100001	10100011011000	10000000000000	10000000000000	11111111111111	xxxxxxxxxxxxxx
E5b-I	11010000001000	10100110010010	10000000000000	10000000000000	11111111111111	xxxxxxxxxxxxxx
E5b-Q	11010000001000	10001100110001	10000000000000	10000000000000	11111111111111	xxxxxxxxxxxxxx
Summary	1x0x00x0x0x00x	10x0xxxxx1x0xx	10000000000000	10000000000000	11111111111111	xxxxxxxxxxxxxx

Figure 5 shows the hardware architectures of the proposed multi-frequency universal code generator by GNSS. Figure 5 shows universal code generators that can generate GPS signals, BDS signals, GLONASS signals, and Galileo signals, respectively. On reviewing Figure 5, it can be seen that the use of multiplexers and XOR logic was reduced compared to Figure 4 by applying the hardwiring technique. As multiplexer use is reduced, the use of ROMs used for the Feedback ROMs1/2, which store the multiplexer control signals of Feedback Taps1/2, and the Output ROMs 1/2, which store the multiplexer control signals of the Output Taps1/2, can also be reduced. Additionally, in the case of GLONASS, Galileo and BDS, the hardwiring technique can also be applied to Initial ROM. Since the ROM use is reduced by 1 depth per 1 bit width for the bit widths applied by the hardwiring technique, a large amount of ROM use can be reduced in cases where satellite numbers are received as inputs. Therefore, in order to check the reduction rate of unnecessary hardware resources, the normalized multiplexer use, normalized XOR logic use, and normalized ROM use for each of the GNSS shown in Figures 4 and 5 are shown in Table 6. Figure 5a shows the proposed multi-frequency universal code generator for GPS signals, indicating that the use of multiplexers, XOR logics, and ROMs decreased by 43%, 39%, and 4%, respectively, compared to Figure 4a. Figure 5b shows the proposed multi-frequency universal code generator for BDS signals, indicating that the use of multiplexers, XOR logics, and ROMs decreased by 29%, 29%, and 5%, respectively, compared to Figure 4b. Figure 5c shows the proposed multi-frequency universal code generator for GLONASS signals, indicating that the use of multiplexers, XOR logics, and ROMs decreased by 54%, 59%, and 5%, respectively, compared to Figure 4c. Figure 5d shows the proposed multi-frequency universal code generator for Galileo signals, indicating that the use of multiplexers, XOR logics, and ROMs decreased by 73%, 69%, and 7%, respectively, compared to Figure 4d.

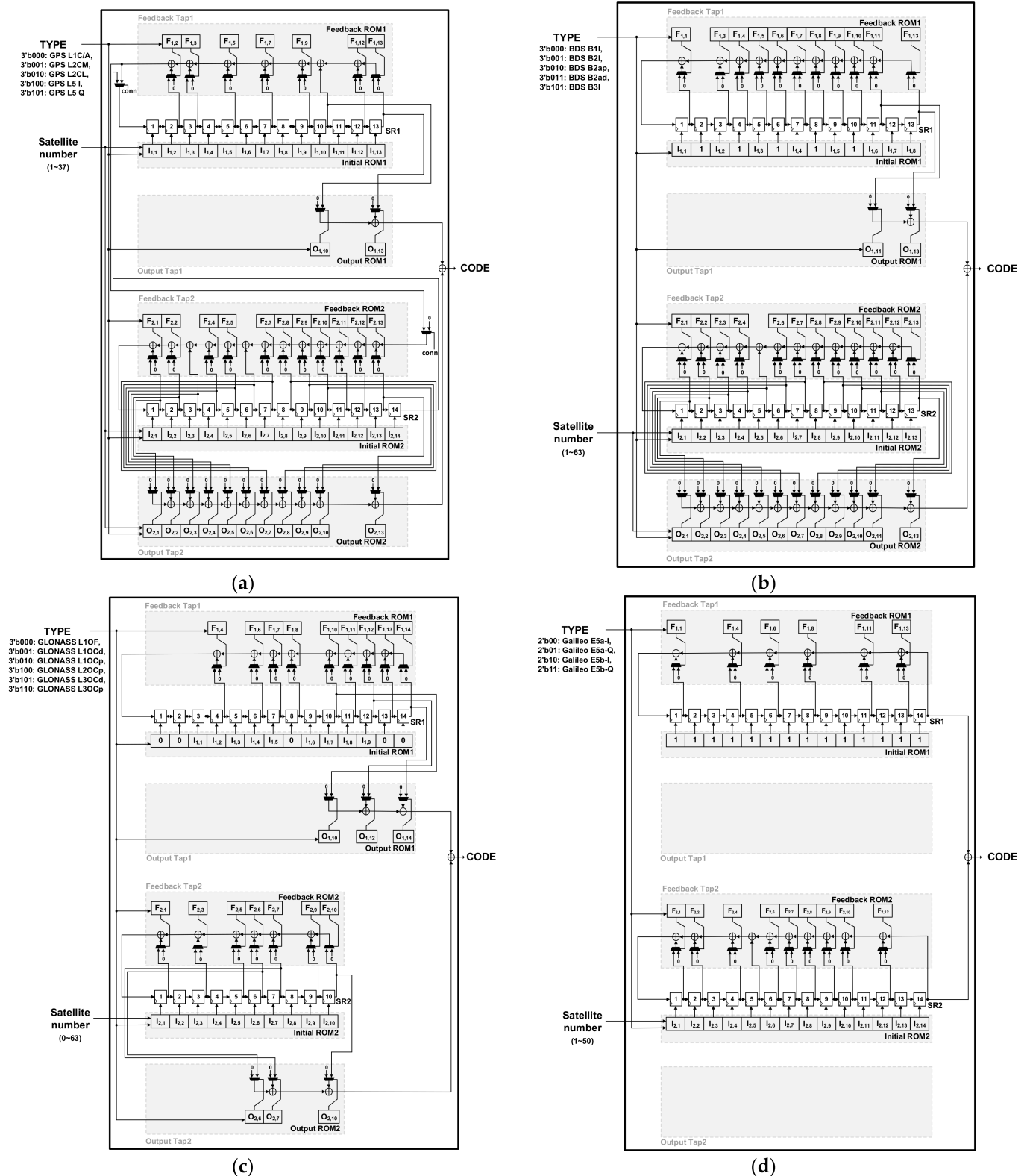


Figure 5. Proposed multi-frequency universal code generator architecture of each GNSS signal. (a) GPS. (b) BDS. (c) GLONASS. (d) Galileo.

Table 6. Comparison of normalized hardware resource use of previous code generator and proposed code generator.

GNSS	Previous [6]/Proposed Universal Code Generator		
	MUX	XOR	ROM
GPS	100%/57%	100%/61%	100%/96%
BDS	100%/71%	100%/71%	100%/95%
GLONASS	100%/46%	100%/41%	100%/95%
Galileo	100%/27%	100%/31%	100%/93%

5. Experimental Results

In the experiment, synthesis and implementation were carried out with Xilinx Vivado 2020.2, and the Kintex Ultrascale KCU105 board was used as the field programmable gate array (FPGA) board. Conventional code generators by GNSS and a previous multi-frequency universal code generator were implemented for comparison with the proposed code generator. All codes generated from conventional, previous, and proposed were the same as the as the code provided from official ICD, implying that all the codes can be used for acquisition and tracking in a GNSS receiver. With the results of the synthesis, the look up tables (LUTs) and registers of the existing code generator and the proposed code generator were compared.

Figure 6 shows a comparison of the normalized hardware resource use of the proposed multi-frequency universal code generator, the previous universal code generator, and the conventional code generators by GNSS, and it can be seen that the hardware complexity was significantly reduced in the proposed multi-frequency universal code generator. As shown in Figure 6a, the LUT use of the proposed multi-frequency universal code generator for GPS signals is reduced by about 13% compared to the previous universal code generator and about 10% compared to the sum of the hardware resource use of the conventional code generators. In addition, since the previous universal code generator and the proposed multi-frequency universal code generator share the shift registers needed to generate the codes, the resistor use is reduced by about 71%. When comparing the hardware resource utilization for BDS, GLONASS, and Galileo signals, it can be seen that in the case of BDS signals, as shown in Figure 6b, the proposed multi-frequency universal code generator reduced LUT utilization by about 11% compared to that of the previous multi-frequency universal code generator and reduced LUT utilization by about 23% and the register utilization by about 78% compared to the sum of the hardware resource utilization of the conventional code generators. In the case of GLONASS signals, as shown in Figure 6c, the proposed multi-frequency universal code generator reduces LUT utilization by about 18% compared to the previous multi-frequency universal code generator and reduces LUT utilization by about 17% and the resistor utilization by about 78% compared to the sum of the hardware resource utilization of the conventional code generators. In particular, in the case of Galileo signals, since the hardwiring technique can be applied to all of Output Tap1, Output Tap2, and Initial ROM1 as shown in Table 5, the proposed multi-frequency universal code generator could save a lot of hardware resources. As shown in Figure 6d, the proposed multi-frequency universal code generator reduced LUT utilization by about 36% compared to that of the previous multi-frequency universal code generator and reduced LUT utilization by about 37% and the register utilization by about 74% compared to the sum of the hardware resource utilization of the conventional code generators. In conclusion, the proposed universal LFSR structure can generate various codes with single hardware that always requires lower hardware resources than existing studies by applying the hardwiring technique.

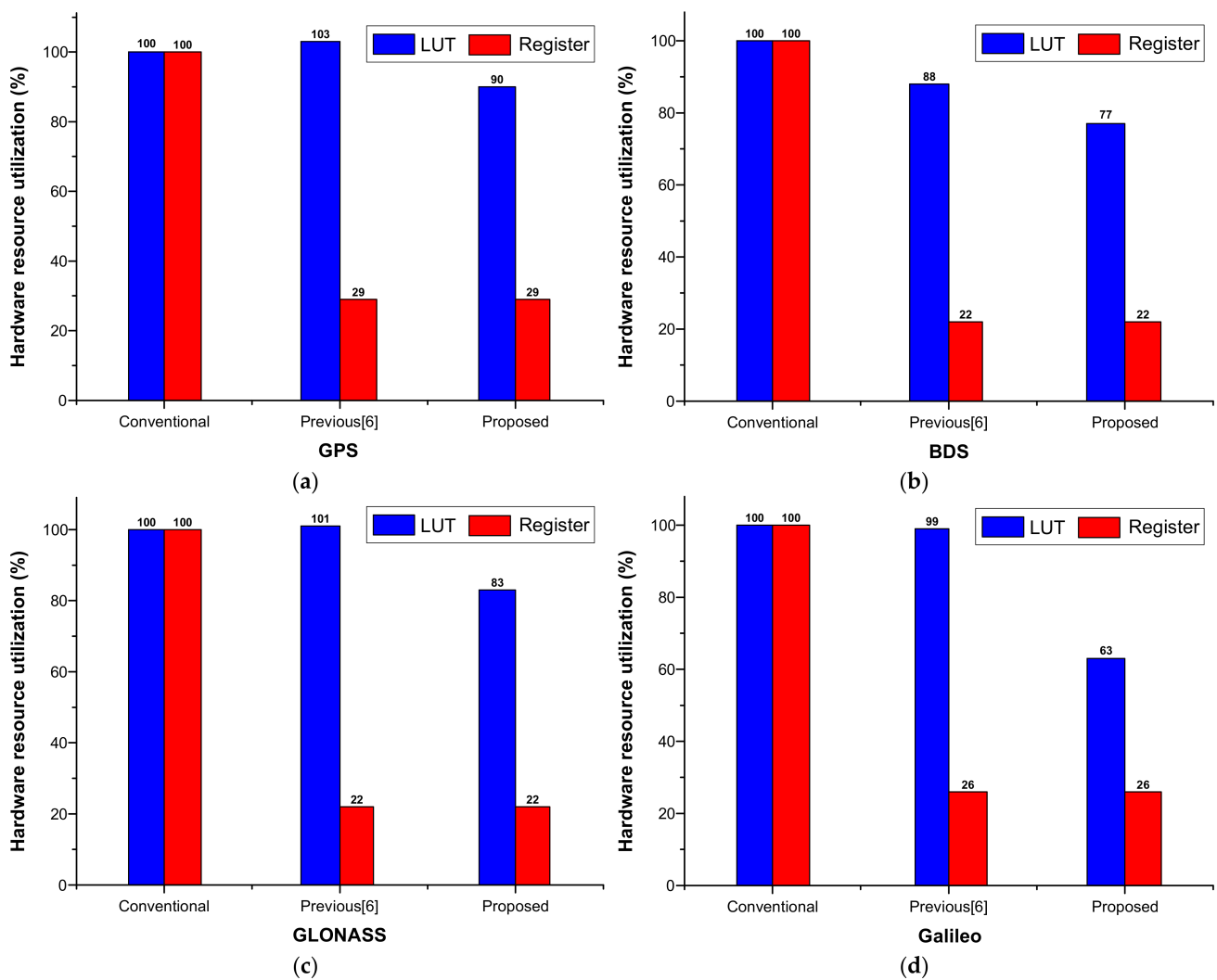


Figure 6. Hardware resource utilization comparison of the proposed multi-frequency code generator for each GNSS. (a) GPS. (b) BDS. (c) GLONASS. (d) Galileo.

6. Conclusions

In this paper, the structure of a universal code generator necessary for the development of multi-frequency receivers was proposed. By applying the hardwiring technique to the feedback polynomials of the existing individual code generators and the common elements of the initial values and output registers, the unnecessary use of multiplexers, XOR logics, and ROMs was reduced as much as possible. Using Xilinx FPGA, the structures of conventional individual code generators, the previous universal code generator [6], and the proposed hardware structure were implemented, and their hardware utilization were compared. Based on this experiment, the proposed LFSR-based universal code generator can save up to 37% of LUT and 78% of register compared to the conventional code generators, and 36% of LUT compared to the previous universal code generator. Therefore, the proposed hardware structure facilitates the implementation of multi-frequency receivers for high precision and high reliability.

Author Contributions: Conceptualization, H.Y.; methodology, M.K., J.P. and H.Y.; software, M.K.; validation, M.K. and H.Y.; formal analysis, J.P., G.J. and H.Y.; investigation, M.K. and G.J.; resources, M.K., J.P. and G.J.; data curation, M.K.; writing—original draft preparation, M.K.; writing—review and editing, J.P. and H.Y.; visualization, M.K., J.P. and G.J.; supervision, H.Y.; project administration, H.Y.; funding acquisition, H.Y. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by Navcours Co., Ltd.

Acknowledgments: This work was supported by Navcours Co., Ltd. and National R&D Program through the National Research Foundation of Korea (NRF) funded by Ministry of Science and ICT (2020M3H2A1078119).

Conflicts of Interest: The authors declare no conflict of interest.

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